b. Status of MuTr FEE Electronics Upgrade
(Itaru Nakagawa, RIKEN/RBRC)

New JSPS funded muon tracker trigger electronics (MuTRG-FEE) was installed in the PHENIX north muon tracker (MuTR) prior to the ongoing Run 9. The new electronics has been operated successfully and detailed studies of the MuTRG-FEE electronics based on Run 9 data are underway. Further detail of offline analysis can be found in the following paragraph. The communication between the backend data collection and data merge (MuTRG-MRG) board and a LL1 trigger processor prototype tile has been also tested successfully. Production of the new MuTRG-FEE boards for the south muon spectrometer was completed by the early Summer 2009. They were fully installed as shown in Fig. 1 throughout summer to fall of 2009 and to be commissioned in Run 10 using Au-Au beams.

Fig. 1 Installed new trigger electronics in South Muon tracker Station-1.

Shown in Fig. 2 is the turn on curve of the trigger efficiency plotted as a function of track momentum evaluated using reconstructed tracks in North MuTR. The trigger threshold is certainly pushed higher to around 8.5 GeV (parameter "p1" in Fig. 2 fit) compared to the maximum threshold limit of about 2 GeV given by MuID. The plateau saturates around the efficiency of 0.9. This is the consequence of the product of the individual efficiencies in each station (about 0.98) and the vertex cut efficiency. Note the efficiency depends on the luminosity. Better efficiency can be achieved by relieving the operating conditions of the trigger electronics such as threshold, acceptance range of track sagitta, with or without strip clustering, AND or OR logic selection of MuTR redundant planes in each stations (MuTR chambers of Station-1, 2, and 3 consisted of 3, 3, and 2 gaps, respectively. New trigger electronics were implemented to 3, 2, and 2 non-stereo planes of these stations, respectively for redundancy.) On the other hand, the higher efficiency would be the trade off between the rejection power. Shown in Fig. 3 is the correlation between the trigger efficiency versus the total rejection power

(BBC⊗MuID⊗MuTrig) evaluated at the BBC rate of 1.5MHz[1]. Plotted data points are the performance of different operating conditions of new trigger electronics as described previously. The achieved efficiency of >0.9 is satisfactory at this BBC rate, which requires only the total rejection power of 750. Such a high efficiency may be degraded at the projected luminosity of 1×10^{32} (expected BBC rate of about 6MHz) for Run11, which requires higher rejection power, i.e. about 3000. However, note these results are still preliminary stage and there are still plenty of rooms to improve the trigger performance. Following items are some ideas to be addressed in future study to retrieve the performance:

- More efficient MuID trigger algorithm
- Track Matching with MuID
- Timing cut by RPC
- Track matching with RPC
- Tighter background shields
- Quenching cross talks in MuTR chamber
- Etc.

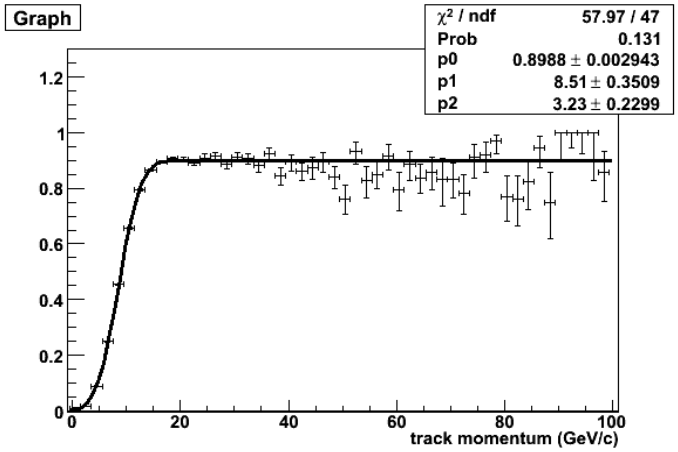

Fig. 2 Turn on curve of the muon trigger as a function of track momentum evaluated from Run9 data in offline analysis.

[1] The BBC rate of 1.5MHz was the one of the highest luminosity run achieved in Run9.

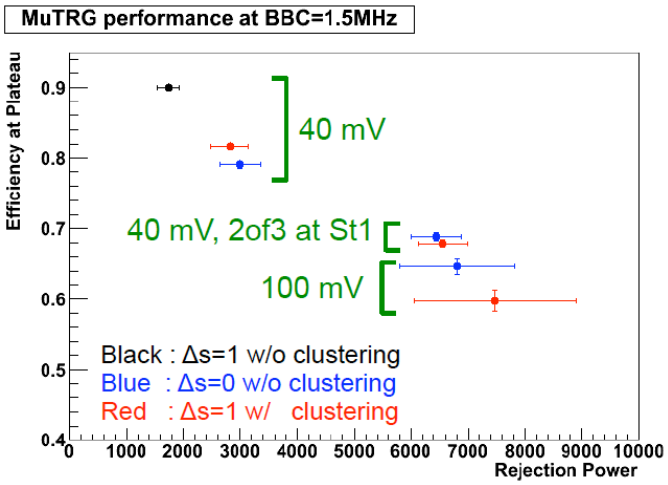

Fig. 3 Correlation between the trigger efficiency vs. rejection power observed at BBC rate of 1.5MHz. 40mV and 100mV are threshold condition applied to the cathode signal at new trigger boards. Δs=1 and 0 represent the acceptance of sagitta range of strip ±1 and ±0 from the central strip of the trajectory.

c. Trigger Electronics
(John Lajoie, Iowa State)

Since the last review development work has continued on the "base" board that will hold up to eight trigger tiles (four required for the Muon Trigger Upgrade). A decision was made to manufacture the base board prototypes (five in total) using a material similar to FR4, instead of the Rogers 4350B material that was used for the trigger tiles. The Rogers 4350B material has a much better high frequency response than FR4, reducing the degradation of high-speed serial signals transmitted on the board. However, this material has a greater coefficient of thermal expansion, and when manufacturing the boards it also demonstrates a greater degree of "slip" between layers when the board is being pressed. In a multilayer board at 9U size, this requires larger tolerances, pads and keep-clear areas than needed with FR4. It would not be possible to manufacture the base board without significant redesign, as well as switching to components with a larger pin spacing. In fact, it was not clear such a board could be manufactured using the FG1136 Xilinx FPGA's.

Based on tests of bit-error rates and signal transmission through varying lengths of FR4, it was concluded that signal quality should be sufficient with the FR4-based board, particularly if use was made of the advanced features of the Xilinx GTPs (transmitter boost and pre compensation, as well as the ability to control the latching of the data within the "eye" diagram). Five base board prototypes were ordered using the FR4 material, and two boards were populated for initial testing.

Initial testing with the base board focused on the required infrastructure to support the VME interface (for PHENIX communication) and the on-board I2C interface to communicate with the trigger tiles. Because the VME interface is entirely contained